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(54) Method and device for dynamically self-biasing regions of integrated circuits

(57) Junction isolation between a second region (2) that is normally clamped at a reference potential, contained within a first region (1) of an opposite type of conductivity whose potential (V1) is subject to large inertial swings is ensured even when the potential of said first region (1) moves toward and beyond the reference potential to which said second region (2) is clamped by clamping said second region (2) to said reference potential by a switch (T) causing the switch (T) to open thus placing the second region (2) in a floating state free to track the potential excursion of the first region (1) and closing again the switch (T) after the potential of the first region (1) has returned to a normal value. A comparator senses a shift of the potential of the second region (2) from the reference potential to which is clamped which is dynamically induded by the capacitive coupling of the two regions, and triggers off the clamping switch (T).

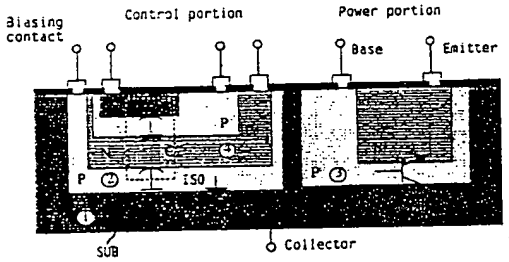

FIG. 1

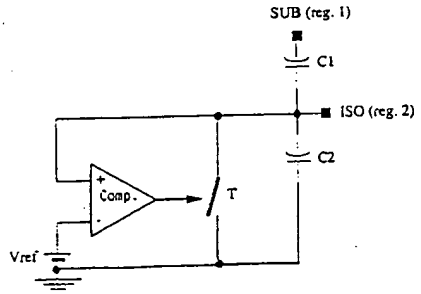

FIG. 2

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Description

The present invention relates to a switching method for self-biasing regions of integrated circuits in order to ensure the maintenance of an effective junction isolation between two different regions coupled with each other also when one of the two regions is subject to large voltage swings and to a wholly integratable device implementing the method. The invention is particularly, though not exclusively, useful in integrated circuit that include power circuits and control circuits integrated on the same chip.

In integrated circuits (IC), output power devices and logic control circuits are often integrated on the same chip. This kind of applications are innumerable: for example IC implementing a so-called "electronic transformer" for driving low-power halogen lamps, driving systems for displays, electric motors, actuators and the like.

Considering an integrated power device, for example a bipolar transistor, a Darlington structure or an equivalent power MOS, having an external reactive load connected to the collector (or drain) node thereof, when the control circuitry switches off the power device, the collector's (or drain's) voltage may assume a negative value (below ground potential). These induced voltages may be extremely dangerous when the power device is integrated together with the control circuits on the same chip.

A family of this type of devices is the one commonly known with the commercial name of VIPower. In these devices, as schematically shown in Fig. 1, the current terminal of an output power device, for example the collector of an NPN transistor, coincides with the substrate (region 1), commonly an N-type semiconductor, of the IC, while a logic control circuitry is integrated within an isolation region (region 2) commonly a P-type diffusion (e.g. a P-well), diffused in the substrate region 1.

Isolation between the substrate-collector (region 1) and the isolation region (region 2) is ensured by the reverse bias of the P-N junction between the two regions.

Under normal working conditions of the IC, the isolation region (P-well) containing control circuitry, is customarily connected to a certain reference voltage, which in a case as the one depicted in Fig 1, may be the lowest potential available, in practice to ground potential. In this type of architecture, during operation, the N-type substrate region which coincides with the output current terminal of the power device, in the example shown the collector of an NPN power transistor, is always at a positive voltage as referred to ground potential. Therefore the intrinsic parasitic transistors of the integrated structure are inhibited.

If, for any reason, for example following the switching off of the power device, the N-type substrate region assumes a negative voltage (below-ground) of a negative value greater than the conduction threshold, the parasitic transistors of the integrated structure turn on and absorb current from the region containing the control circuitry. This may cause malfunctioning of the control circuits as well as of the controlled power devices.

These risks could be easily eliminated by biasing the P-type isolation region (P-well) at a potential sufficiently more negative than the maximum negative voltage that may be reached by the N-type substrate region. However, negative bias voltage sources are not normally available and would need to be purposely implemented in the IC.

For simplicity of description, in the ensuing description reference will be made almost exclusively to the sample case of an integrated architecture of the type depicted in Fig 1, based on a P-type isolation region, diffused in an N-type substrate. However it should be understood that similar considerations may be made for a "dual" situation of an architecture using inverted conductivity types and polarities. Moreover, it will be clear to the reader that the technical problems addressed by the present inventors may be encountered in a variety of other types of integrated circuits.

In the past, there have been several proposals for preventing the occurrence of a direct biasing of the junction between two regions coupled together.

French Patent Application No. 89/16144, filed on November 29, 1989, in the name of SGS-THOMSON MICROELECTRONICS and SIEMENS AUTOMOTIVE and US Patent No. 5,382,837, corresponding to the European patent application No. 91850287.8, filed on June 27, 1991, by the same applicant of the present application, describe circuit arrangements for ensuring junction isolation between two regions.

Both these known proposed solutions propose to clamp a P-type isolation region to ground potential through a first switch as long as an N-type substrate region remains at a positive voltage and to connect the isolation region to the substrate region by a second switch when the latter region assumes a negative (below-ground) potential.

These known solutions, beside requiring the use of two switches have critical aspects and drawbacks. A first disadvantage is represented by the need of ensuring with absolute reliability that the two switches may never be conductive simultaneously, because this would short-circuit the substrate region to ground. A second difficulty is in ensuring a timely biasing of the isolation region at the substrate potential when the substrate's voltage drops abruptly toward a negative (below-ground) potential.

Therefore there is a need and/or utility for a simpler and more reliable switching or self-biasing method and device capable of ensuring a timely response in case of abrupt voltage changes of a first region, for example a substrate region, toward the voltage at which is normally biased a second region, for example an isolation region, in order to prevent any possibility of direct biasing the junction between the two regions.

These objectives are fully met by the method and the device of the present invention.

The method of the invention is based on maintaining the second region clamped at an available reference potential by a switch and commanding the opening of the switch, thus placing the region in a high impedance condition as referred to the node at said reference voltage to which is normally connected through the switch. The opening of the switch occurs automatically in response to a variation toward said reference potential of the voltage of the first region of a gradient sufficient to cause, by a capacitive dynamic voltage distribution, a momentary shift in the same direction of the voltage of the second region.

In other words, the method implies the interruption of the connection of the second region to the clamp voltage node, thus allowing the second region to float and track, by virtue of its capacitive coupling the voltage swing of the first region, which is subject to abrupt voltage changes toward said clamp voltage.

By effect of the capacitive coupling and therefore of a dynamic voltage distribution, when an abrupt voltage variation of the first region toward the reference potential to which the second region is clamped occurs the second region is momentarily subject to a voltage shift from the clamping reference voltage of the node to which is connected through the switch in the same direction of the variation (dV/dt) of the voltage of the first region; thus the second region assumes momentarily a potential lower (or greater in a dual situation with inverted polarities) then the reference voltage to which is clamped. This momentary shift eventually causes the opening of the switch and thus permits to the potential of the second region to continue to track (in a floating state) the voltage change (dV/dt) of the first region by virtue of the capacitive coupling existing therebetween, thus making impossible the occurrence of a direct biasing of the junction between the two regions.

Of course, the system is capable of reacting in the above-described manner, only in presence of a gradient of variation of the voltage of the first region (dV/dt) of a sufficient magnitude. On the other hand, in systems operating in a switching mode, the changes of state are typically step-functions (that is extremely abrupt) and therefore the magnitude of the gradient of the voltage variation is generally sufficient.

In practice, the dynamic self-biasing switching device of the invention may consist of a single integrated switch capable of establishing a connection of the second region with a node at a reference voltage and a controlling comparator.

The different aspects and advantages of the invention will become even more evident through the following description of several important embodiments, included herein for purely illustrative and non limitative purposes, and by referring to the annexed drawings, wherein:

Figure 1 shows the architecture of an integrated circuit for single supply wherein the above-identified technical problems may be encountered;

Figure 2 is a diagram of the device of the invention;

Figures 3 and **4** show a dual situation of the one depicted in Figures 1 and 2;

Figure 5 is a basic circuit diagram of an embodiment of the invention;

Figure 6 is a basic circuit diagram according to an alternative embodiment of the invention;

Figure 7 is a complete circuit diagram of a device of the invention;

Figure 8 shows circuit's voltage signals obtained by simulation.

A common architecture of an integrated circuit comprising a power section and a control section is schematically depicted in Fig. 1. In the example shown, the power section is represented by a bipolar NPN power transistor having a vertical current flow, the collector of which coincides with an N-type substrate region 1 of the integrated circuit.

The control section, typically a logic circuitry, is realized within a P-type isolation region 2(P-well) diffused in the N-type substrate. In Fig. 1 are symbolically shown the junction capacitance C1 between the substrate 1 and the isolation region 2, the other structural capacitances of the integrated architecture of the control circuitry, toward a common ground node, indicated as a whole with C2, as well as the NPN power transistor and the junction (diode) between the substrate 1 and the isolation region 2.

For an application of the type schematically represented in Fig. 1, the basic diagram of the device of the invention is shown in Fig. 2.

The capacitance C1 represents the junction capacitance between the N-type substrate 1 (SUB) and the P-type isolation diffusion 2 (ISO). The capacitance C2 represents the series of capacitances relative to the junctions between regions of different type of conductivity that realize the integrated structures of the components of the control circuitry contained in the isolation region 2.

In the examples of Figures 1 and 2, the substrate 1 constitutes the collector of an NPN power transistor. During normal operation, the substrate-collector 1 (SUB) of the integrated circuit is at a positive voltage as referred to a common ground potential of the circuit, to which the emitter of the same NPN power transistor as well as the emitter of a generic NPN transistor of the control section of the integrated circuit may be coupled, as depicted in Figures 1 and 2.

According to the basic scheme of Fig. 2, the isolation p-well region 2 (ISO) is connected, through a switch T to the ground node of the circuit.

As long as the potential of the region 2 coincides with the ground potential, the comparator COMP maintains the switch T closed.

When for any reason, as for example because of the switching off of the output power transistor and in presence of an inductive external load, the potential of the region 1 (SUB) drops abruptly toward ground poten-

tial (being trendily dragged inertially toward negative voltage values), by capacitive coupling also the potential of the isolation region 2 (ISO) is momentarily dragged toward negative (below-ground) voltage values. Such a dynamic potential shifting of the isolation region 2 beyond the reference voltage (ground potential) to which is clamped by the switch T, in the example shown toward a negative voltage, is detected by the comparator COMP which changes state thus opening the switch T.

The opening of the switch T places the isolation region 2 (ISO) in a floating or high-impedance condition with reference to the ground node so that the region potential is free to track the falling voltage of the substrate region 1, by assuming more and more negative voltage values, because of its capacitive coupling through C1 and C2. This dynamic potential tracking mechanism ensures that the isolation region 2 (ISO) remains always at a more negative potential than the potential assumed by the substrate region 1 (SUB).

The negative voltage value (V2) eventually reached by the isolation region 2 following a negative variation (negative dV/dt) of the voltage V1 of the substrate region 1, is tied to the relative values of the coupling capacitances C1 and C2 and to the value of an eventual leakage current.

By neglecting any leakage current, the following relationship holds:

$$V2=-\frac{C1}{C1+C2}V1 \qquad (1)$$

On the other hand, the period of time during which the isolation region 2 remains at a negative voltage V2 dynamically reached because of its capacitive coupling is tied to the leakage current beside to the actual values of the coupling capacitances C1 and C2. By supposing a leakage current i of a constant value, such a period of time may be calculated with the following equation:

$$T=\frac{V_2}{i}(C1+C2) \qquad (2)$$

Of course, such a period of time T must be sufficiently longer than the maximum interval of time during which the substrate region 1 may assume a negative (below-ground) voltage. Such a maximum period of time may be easily established in the design stage by knowing the electrical characteristics of the external load.

It may be easily verified that, in the majority of cases, the levels of leakage current are sufficiently low so as to make the junction capacitances C1 and C2 of the region 2 quite appropriate for the purpose. The need of increasing the values of the coupling capacitances, by eventually integrating parallel capacitances could present itself only in case the level of leakage currents would be so high as to make the "hold" time T too short.

In practice, in the majority of cases, the device of the invention will not require any externally connected additional component (for example capacitors to be connected in parallel to the intrinsic junction capacitances C1 and C2 of the integrated structure).

Independently of the amplitude of the voltage swings toward negative values by part of the substrate region 1 (SUB) and, by dynamic capacitive voltage distribution by part of the region 2 (ISO) as well, as soon as the potential of the region 2 (ISO) by rising back again toward positive voltages, equals the threshold voltage V_{ref}, which may be predefined so as to be lower than the conduction threshold of the junction between the regions 1 and 2, the comparator (COMP) switches thus closing again the switch T and re-establishing the clamping to ground potential of the region 2.

Figures 3 and 4 show an application of the device of the invention in the case of an equivalent "dual" architecture of the integrated circuit, that is wherein the type of conductivities and polarities are all reversed. Of course, in such an alternative embodiment, the logic of the comparator COMP will also be inverted so as to command the opening of the switch T following a positive dV/dt variation of the voltage of the substrate region 1 (which is normally negative).

For the case of Figures 1 and 2, the basic electric scheme of the arrangement of the invention may be as shown in Fig. 5. The current generator I and the transistors T1 and T2, form an error amplifier, the voltage reference of which is placed to ground potential, while the switch (T in the scheme of Fig. 2) is implemented by the transistor T3.

Upon a negative dV/dt variation on the node of region 1, the node of region 2 assumes a potential that, in first approximation, is given by the equation (1), thus causing the saturation of the transistor T2 and therefore the turning off of the switch T3. In this way, the node coinciding with the region 2 presents an extremely high impedance. At the end of a period of time T given, in first approximation, by the equation (2) or upon a positive dV/dt variation of the voltage of the region 1, the potential of the region 2 rises again toward ground potential.

When it reaches ground potential, the transistor T2 exits saturation thus switching on again the switch T3 which re-establishes a connection of the region 2 to the ground node.

In order to avoid overloading the output of the comparator and therefore obtaining an improved switching performance, the circuit of Fig. 5 may be advantageously modified as shown in Fig. 6.

By adding a stage formed by the transistor T4, the current absorption from the comparator is reduced by a number of times equivalent to the current gain of the stage T4 and, by virtue of the resistance R, the time necessary to effectively clamp the region 2 to ground potential may be considerably reduced because the transistor T3 is already biased when the potential of the region 2 tends to rise above ground potential (that is starts to be driven toward a positive voltage).

A complete circuit scheme of a device of the invention is depicted in Fig. 7.

As can be noted from the scheme, an error amplifier with emitter input and an output stage for driving the isolation region (2) node may be easily identified.

Two diodes, namely: Q93 and Q52, have been added in the circuit of the error amplifier in series with the emitters of the input transistors Q4 and Q5 in order to increase the maximum absolute voltage value that may be reached by the isolation region 2. The resistors in parallel to the base emitter junctions of the input pair of transistors Q4 and Q5 have the function of reducing the storage time thereof.

Finally, the static biasing of Q5 has the function of preventing an excessively deep saturation thereof when conducting.

Voltage diagrams of the node coinciding with a substrate region 1, and of the node coinciding with an isolation region 2, obtained by simulating the use of a switching circuit as the one depicted in Fig. 7 are shown in Fig. 8.

The simulations have fully confirmed the effectiveness of the device of the invention. From the simulations, it has been found that the maximum operative voltage of the node coinciding with the region 1 (substrate-collector) and therefore the range of application of the device of the invention is a function of the amplitude of the gradient dV/dt, to which the same region 1 may be subject, of the capacitive voltage distribution that may be altered in the design stage by realizing capacitances in parallel to the intrinsic junction capacitances C1 and C2 (or by eventually connecting external capacitors), as well as of the open circuit collector emitter breakdown voltage (BVceo) of the integrated components. This last parameter will in fact determine the maximum value (modulus) that may be reached by the voltage of region 2.

According to common fabrication processes of this type of devices, the BVceo of integrated transistors is of about 60V. Should the voltage of the region 2 reach the breakdown voltage of the components, a breakdown phenomenon would be triggered. Such a phenomenon, by injection of current from the ground node toward the region 2 according to equation (2), would reduce the time T with the risk of failing to ensure a junction isolation between the regions 1 and 2. Of course, other parameters that may critically affect the switching process of the invention may be suitably sized in the design stage by taking into account the above-mentioned limits.

Claims

1. A method of dynamically biasing a second region (2) of a first type of conductivity, normally clamped at a reference potential, contained within a first region (1) of a second type of conductivity whose potential (V1) is subject to changes, in order to maintain a reverse bias on the junction between said regions (1, 2) even when the potential (V1) of said first region (1) undergoes an abrupt change toward said reference potential that could eventually lead to directly bias said junction, which comprises

   clamping said second region (2) to said reference potential through at least a switch (T);
   opening said switch (T) thus placing said second region (2) in a high impedance condition as referred to the node at said reference potential in response to a variation toward said reference potential of the potential (V1) of said first region (1) sufficient to cause, by dynamic capacitive voltage distribution, a voltage shift of the potential (V2) of said second region in the same direction;
   closing again said switch (T) upon a discharge of said second region (2) from the potential assumed by said capacitive coupling caused by a leakage current toward the node at said reference potential or in response of a variation in an opposite direction of the potential (V1) of said first region (1) sufficient to cause, by dynamic capacitive voltage distribution a return of the potential (V2) of said second region (2) to said reference potential.

2. The method according to claim 1, wherein said first region (1) is an N-type substrate region and said second region (2) is a P-type isolation region.

3. The method according to claim 1, wherein said reference potential is a common ground node potential.

4. The method according to claim 3, wherein the opening of said switch (T) is commanded upon the dropping of the potential (V2) of said second region (2) below a positive threshold voltage (V_{ref}) referred to ground potential.

5. The method according to claim 1, wherein said regions (1, 2) are regions of an integrated circuit comprising at least an integrated vertical type power device which employs said first region (1) as an output current terminal and which comprises at least a logic control circuitry contained in said second region (2).

6. A device for dynamically biasing a second region (2) of a first type of conductivity of an integrated circuit which is normally biased at a reference voltage and is contained in a first region (1) of a second type of conductivity, which constitutes an output current node of at least a power device, characterized by comprising

   an integrated switch (T) connecting said second region (2) to a node at said reference voltage;

a comparator (COMP) for opening said switch (T) thus placing said second region (2) in a high impedance condition as referred to said reference voltage node, in response to a variation toward said reference voltage of the voltage (1) of said first region (1) sufficient to cause, by dynamic capacitive voltage distribution, a shift in the same direction of the potential (V2) of said second region (2) from said reference voltage.

7. The device according to claim 6, wherein the change of state of said comparator (COMP) occurs upon the crossing in a direction or in the opposite direction of a threshold voltage (V_{ref}) as referred to said reference voltage.

8. The device according to claim 6, wherein said first region (1) is an N-type substrate region and said second region (2) is an isolation P-type region, diffused in said substrate region (1) and said switch (T) is opened by said comparator (COMP) upon a variation of the voltage (V1) of said first substrate region (1) from a positive value toward a negative (below-ground) value.

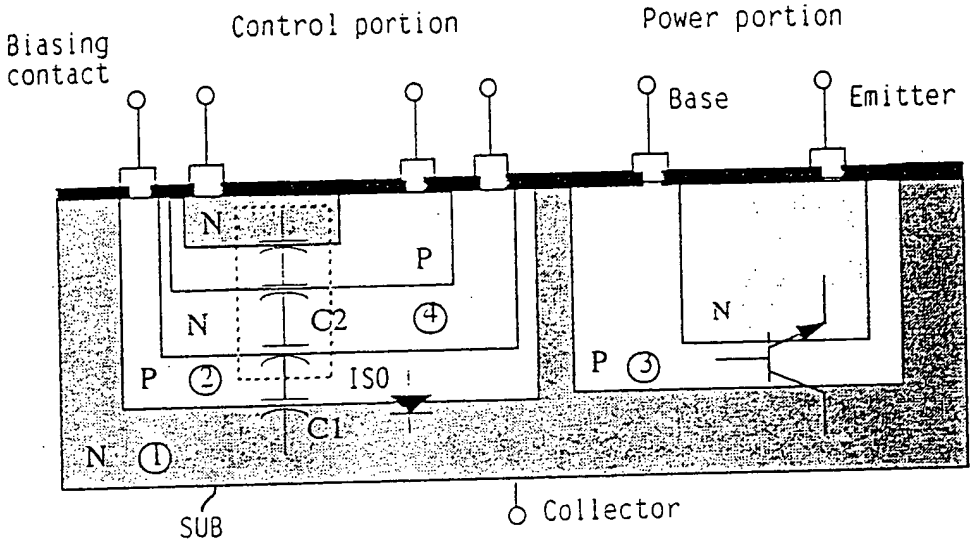

Biasing contact
Control portion
Power portion
Base
Emitter
N
P
N
C2
4
P
2
ISO
C1
N
1
N
P
3
SUB
Collector

FIG. 1

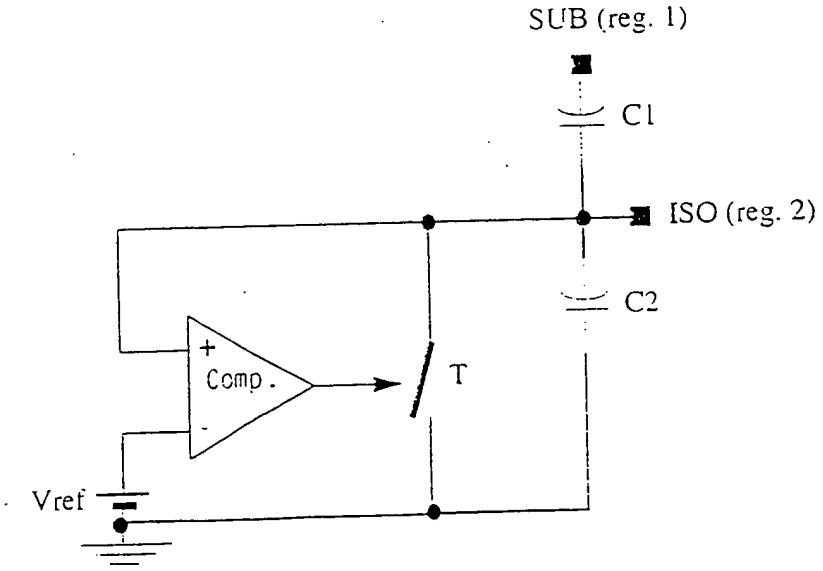

SUB (reg. 1)
C1
ISO (reg. 2)
C2
+
Comp.
-
T
Vref

FIG. 2

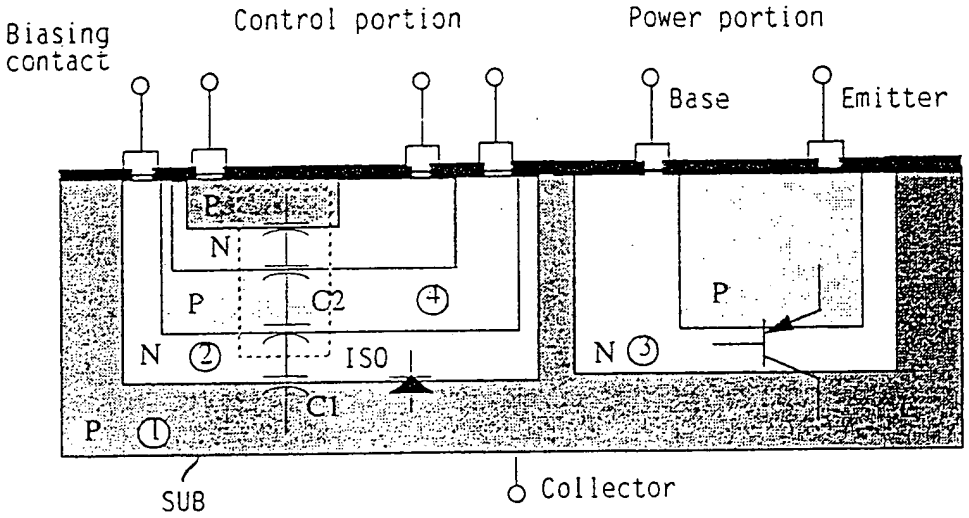

Biasing contact
Control portion
Power portion
Base
Emitter
P
N
P
C2
N
2
ISO
C1
P
1
N
3
P
SUB
Collector

FIG. 3

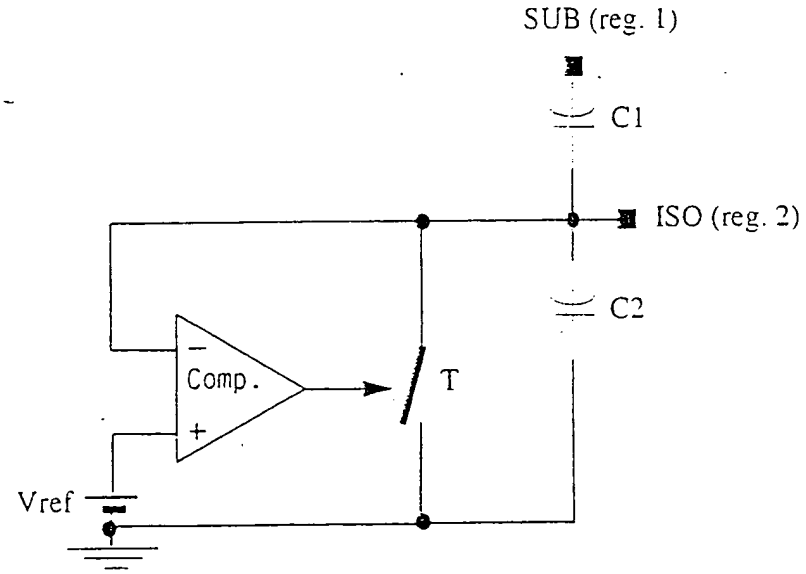

SUB (reg. 1)
C1
ISO (reg. 2)
C2
Comp.
T
Vref

FIG. 4

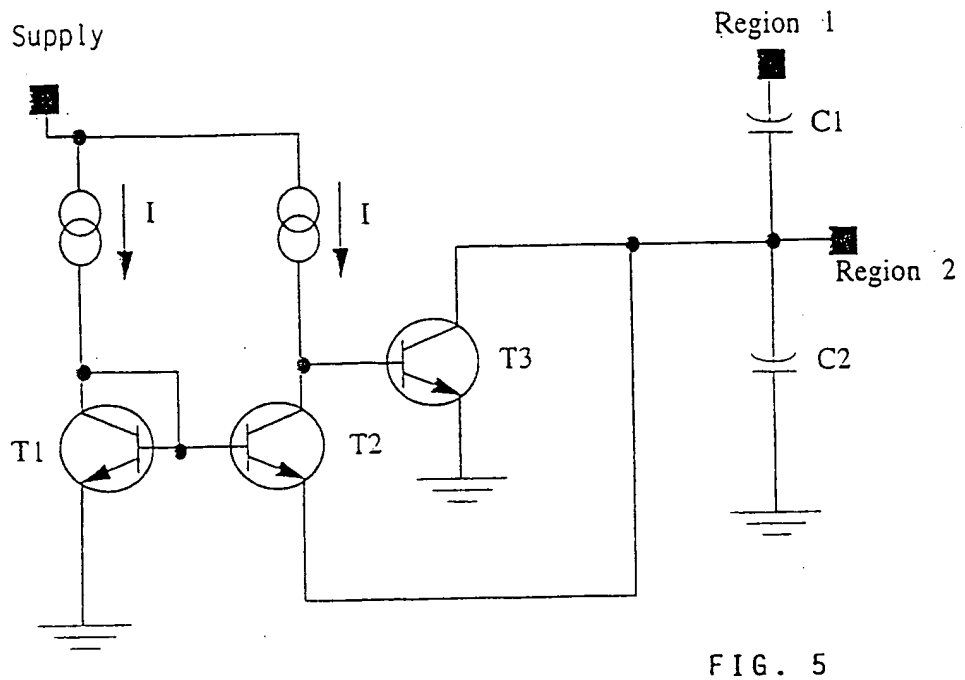

Supply
Region 1
C1
I
I
Region 2
T3
C2
T1
T2

FIG. 5

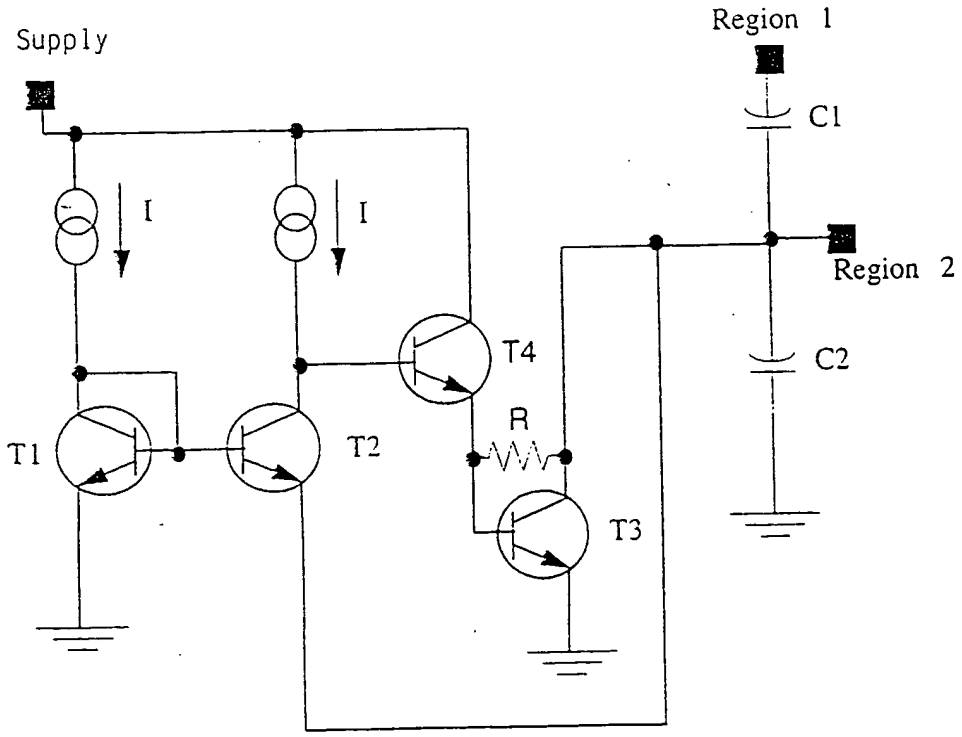
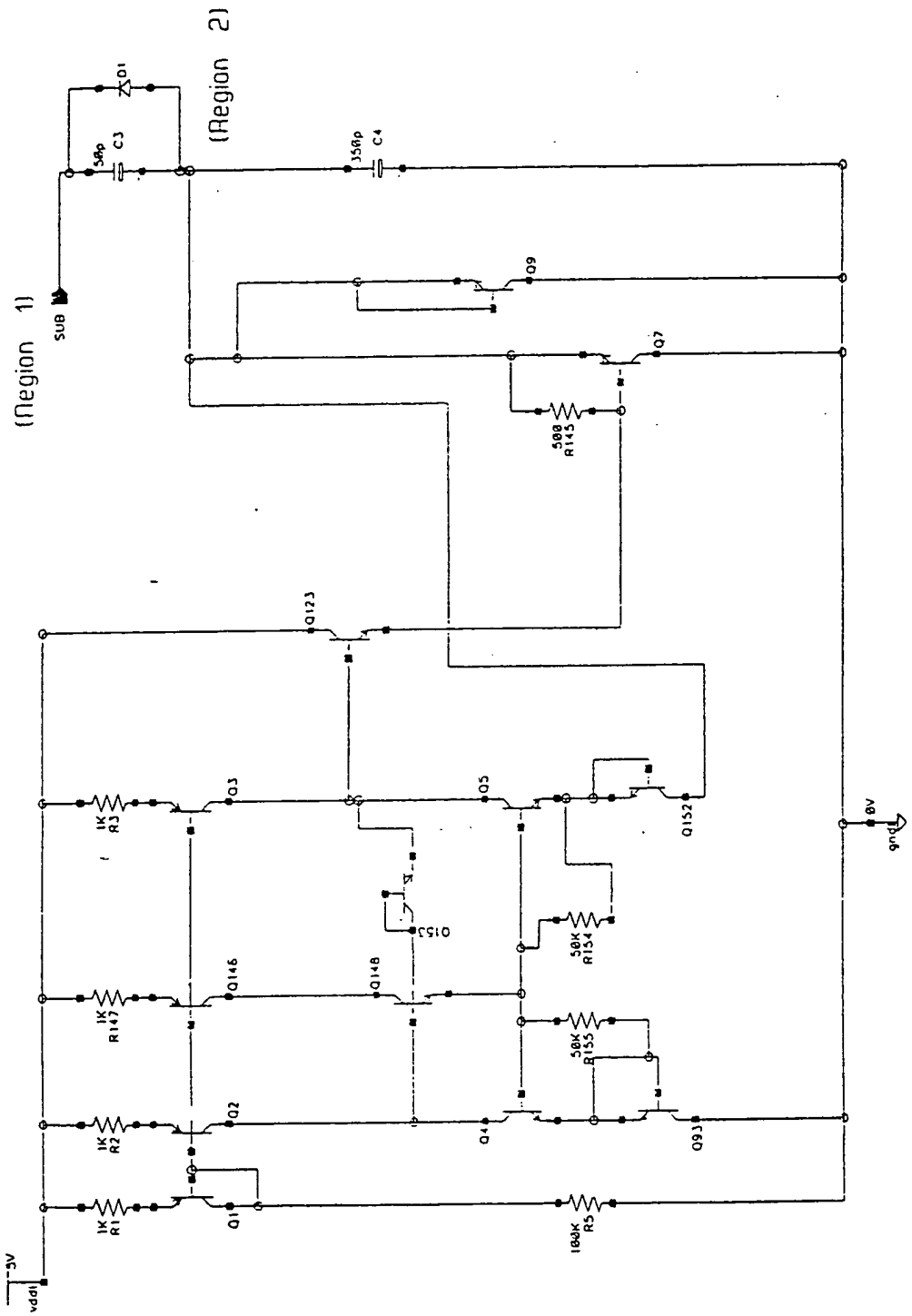

Supply
Region 1
C1
I
I
Region 2
T4
C2
R
T1
T2
T3

FIG. 6


(Region 1)
(Region 2)
SUB
D1
C3
5Ap
C4
35Ap
Q9
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R147
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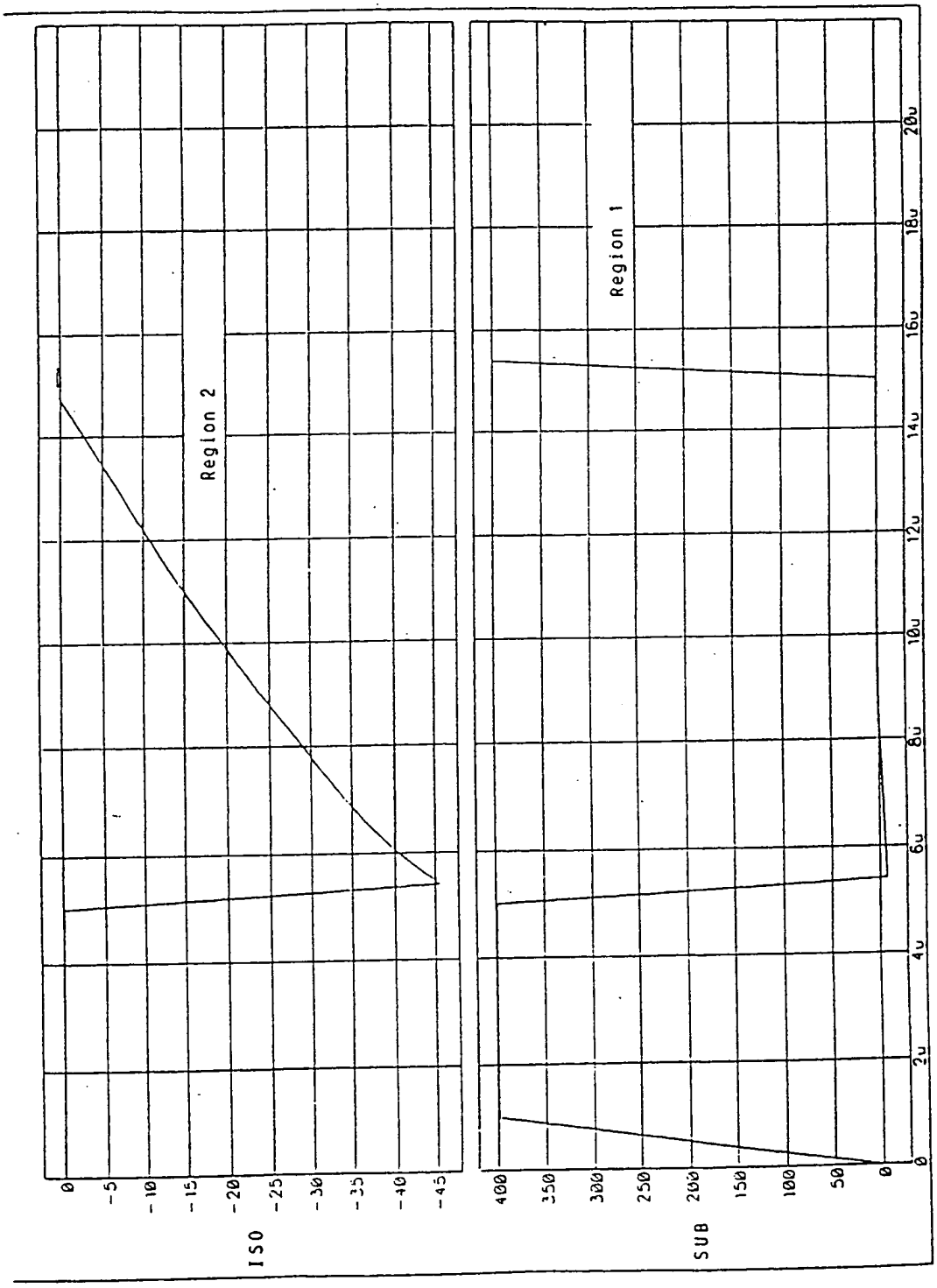
FIG. 7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ISO
SUB
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300
250
200
150
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50
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2u
4u
6u
8u
10u
12u
14u
16u
18u
20u

FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0109

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	EP-A-0 432 058 (SGS THOMSON MICROELECTRONICS ;SIEMENS AUTOMOTIVE SA (FR)) 12 June 1991 * claim 1; figure 4 * ---	1-3	H01L29/00 H01L27/02
A	PATENT ABSTRACTS OF JAPAN vol. 013 no. 522 (E-849) ,21 November 1989 & JP-A-01 212463 (MITSUBISHI ELECTRIC CORP) 25 August 1989, * abstract * -----	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 September 1995	Fransen, L

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